FIRST YEAR OF BACHELOR OF SCIENCE MINOR PHYSICS REVISED SYLLABUS ACCORDING TO CBCS NEP2020

COURSE TITLE:-DIGITAL ELECTRONICS & ARCHITECTURE - SEMESTER-I
W.E.F. 2023-2024

RECOMMENDED BY THE BOARD OF STUDIES IN PHYSICS
AND
APPROVED BY THE ACADEMIC COUNCIL

Devrukh Shikshan Prasarak Mandal's
Nya. Tatyasaheb Athalye Arts, Ved. S. R. Sapre Commerce, and Vid. Dadasaheb Pitre Science College (Autonomous), Devrukh. Tal.Sangmeshwar, Dist. Ratnagiri-415804, Maharashtra, India

Academic Council Item No: **<u>03 dated 8 July 2023</u>**

Name of the Implementing Institute	:	Nya. Tatyasaheb Athalye Arts, Ved. S. R. Sapre Commerce, and Vid. Dadasaheb Pitre Science College (Autonomous), Devrukh. Tal. Sangmeshwar, Dist. Ratnagiri-415804,
Name of the Parent University	:	University of Mumbai
Name of the Programme	:	Bachelor of Science
Name of the Department	:	Physics
Name of the Class	:	First Year
Semester	:	First
Paper	:	I
No. of Credits	:	02
Title of the Course	:	Digital Electronics and Architecture
Course Code	:	S104PHT
Name of the Vertical in adherence to NEP 2020	:	Minor
Eligibility for Admission	:	Any 12^{th} Pass seeking Admission to Degree Programme in adherence to Rules and Regulations of the University of Mumbai and Government of Maharashtra
Passing Marks	:	40%
Mode of Assessment	:	Formative and Summative
Level	:	UG
Pattern of Marks Distribution for SEE and CIA	:	60:40
Status	:	NEP-CBCS
To be implemented from Academic Year	:	2023-2024
Ordinances /Regulations (if any)		

Syllabus for First Year of Bachelor of Science

(With effect from the academic year 2023-2024)

SEMESTER-I **Paper No.– Minor(CS) – I**

Course Title: Digital Electronics & Architecture **No. of Credits - 02**

Type of Vertical: Minor **COURSE CODE: S104PHT**

Learning Outcomes Based on BLOOM's Taxonomy:

After completing the course, the learner will be able to…

Course Learning Outcome No.	Blooms Taxonomy	Course Learning Outcome
CLO-01	Remember	Know all the logic gates, architecture of a computer & purpose of the microprocessor and peripherals
CLO-02	Understand	Understand the working of the basic processing unit of a computer
CLO-03	Apply	Appreciate the instruction sets and types the programming languages
CLO-04	Analyze	Differentiate various types of computers and peripherals
CLO-05	Evaluate	Demonstrate the working of various digital circuits using simulators
CLO-06	Create	Draw the memory map of a computer

Syllabus for First Year of Bachelor of Science

(With effect from the academic year 2023-2024)

SEMESTER-I **Paper No.– Minor(CS) – I**

Course Title: Digital Electronics & Architecture **No. of Credits - 02**

Type of Vertical: Minor **COURSE CODE: S104PHT**

COURSE CONTENT			
Module	**Content**	**Credits**	**No. of Lectures**
1	**Logic circuits & functions:** Combinational circuits & functions: Basic logic gates & functions, D'Morgan Laws, truth tables. Synthesis of logic functions with basic gates, SOP and POS, Minimization. Fan-in & fan-out concept; tristate buffers, Half & full adder, Encoder, Decoder, Flip-flops, Gated S-R and D latches, edge-triggered D-FF, JK FF. Counters and Shift registers. Number/character representation. **Computer Abstractions:** Structure and operation of a computer, functional units & their interaction. **Sequential circuits and functions:** State diagram and state table; finite state machines and their synthesis.	**01**	**15**
2	**Instruction set architectures:** Memory organization, addressing & operations; word size, big & little-endian arrangements. Instructions, sequencing. Instruction sets for RISC and CISC Operand addressing modes; pointers; indexing for arrays. Machine language, assembly language, assembler directives. Function calls, processor runtime stack, stack frame. Types of machine instructions: arithmetic, logic, shift, etc. Instruction sets, RISC and CISC examples. **Basic Processor Unit:** Main components of a processor: registers and register files, ALU, control unit, instruction fetch unit, and interfaces to instruction and data memories. Datapath. Instruction fetch and execute; executing arithmetic/logic, memory access and branch instructions; hardwired and micro-programmed control for RISC and CISC. **Basic I/O:** Accessing I/O devices, data transfers between processor and I/O devices. Interrupts and	**01**	**15**

	exceptions: interrupt requests and processing.		
	Total	**02**	**30**

Note:- The introductory and demo/practical oriented portion of most of the topics will be taught in flipped classroom mode.

Reference book:
Carl Hamacher et al., Computer Organization and Embedded Systems, 6 ed., McGraw-Hill 2012
Text book:
Techmax publication book

Additional References:
Patterson and Hennessy, Computer Organization & Design, Morgan Kaufmann, 2011
R P Jain, Modern Digital Electronics, Tata McGraw Hill Education Pvt. Ltd. , 4th Edition, 2010

Access to the Course

The course is available for all the students admitted for Bachelor of Science.

Methods of Assessment

The assessment pattern would be 60:40, 60% for Semester End Examination (SEE) and 40% for Continuous Internal Assessment (CIA). The structure of the SEE and CIA would be as recommended by the Board of Studies and approved by the Board of Examination and the Academic Council of the college.

Pattern of Evaluation

The Examination/Evaluation pattern shall be framed by the Board of Examination with its final approval from the Academic Council of the College.